ABSTRACT OF THE DISCLOSURE

An architecture and method for dynamic resource allocation and scheduling in a communication device is disclosed herein. The method of controlling hardware resources in a communication device having a processor, a computer readable memory, and at least one hardware resource coupled to each other includes several steps. The first step locates a memory address in the computer readable memory that is associated with a first hardware resource. In the next step, control information associated with the first memory address is transmitted to the first hardware resource for it to be operated. In the last step, a pointer associated with the first address that locates a subsequent address for a subsequent hardware resource, is read.